We Claim:

1. A boundary scan interface circuit for use with a test access port (TAP) controller for testing the state of pin drivers of an IEEE 1149.1-compliant integrated circuit (IC) having a boundary scan register, said interface circuit comprising:

a tristate control circuit for selectively controlling pin driver enable input of said pin drivers and responsive to a control input for temporarily de-asserting a signal that tri-states the pin drivers during a capture cycle of said TAP in which pin logic values are captured by the BSR.

2. An interface circuit as defined in claim **1**, further including:

an update control circuit responsive to a second control input for generating a boundary scan cell update signal to provide a first test mode for loading test data into a boundary scan register without updating outputs of said register.

3. An interface circuit as defined in claim **2**, said IC having first and second storage registers for storing first and second control bits.

4. An interface circuit as defined in claim **1**, said tristate control circuit including:

first means for combining a TAP Capture-DR state signal and a control input and producing a tristate disabling control signal ; and

second means for combining a tristating signal and said tristate disabling control signal for producing a pin driver enable control signal.

5. An interface circuit as defined in claim **4**, said tristate disabling control signal being a pulse having a duration of one clock period of a test clock.

6. An interface circuit as defined in claim **2**, said update control circuit including means for combining a test clock signal and a TAP Run-test/idle state signal for producing a delayed update control signal; and

means responsive to a test mode control signal for selecting between a TAP Update-DR state signal and said delayed update control signal for providing an update signal to said BSR.

7. An interface circuit as defined in claim **6**, said update control circuit including:

means for combining a test clock signal with one of a TAP run-test/idle signal and a TAP select-DR signal to produce a delayed boundary scan register update control signal; and

a selector responsive to a test mode control signal for selecting between a test access port update signal and said delayed control signal.

8. A method for testing the function of a pin driver enable bit of unconnected pins of an integrated circuit (IC) having a boundary scan register (BSR), comprising:

loading the BSR with pin driver data and enable logic values and updating BSR outputs;

re-loading the BSR with data, without updating BSR latches, that would cause the output drivers to drive their opposite logic value and to tristate their outputs;

applying an output driver tristating signal to tristate all pins simultaneously;

updating BSR outputs;

de-asserting said tristating signal and then capturing pin logic values into said BSR; and

unloading captured data from said BSR and comparing captured data against expected values.

9. A method as defined in claim **8**, performing said updating BSR outputs during one of a TAP Run-Test/Idle state or a TAP Select-DR state of an IEEE 1149.1 test access port (TAP).

10. A method as defined in claim **8**, performing said step of de-asserting said tristating signal in response to a delayed test access port (TAP) Capture-DR signal and an active test mode control signal.

11. A method as defined in claim **8**, performing said step of tristating all pins simultaneously prior to said loading the BSR with pin and pin driver enable logic values and maintaining said pins continuously tristated throughout a test and de-asserting the tristating only during a test clock period in which test connection logic values are captured by the BSR.

12. A method of testing an integrated circuit having a boundary scan register (BSR) to determine whether circuit output pins have short circuits between the pins and a power rail, or any defect that might result in the flow of excess current through the pin or a power rail, the method comprising:

tristating said output pins;

loading the BSR with values to force output drivers into desired output states;

capturing pin outputs into said BSR while de-asserting tristating only during a capture cycle; and

unloading captured data from said BSR and comparing captured data against expected values.

13. A method as defined in claim **12**, further including, after said tristating said output pins, configuring said circuit in a test mode in which output pin tristating is de-asserted during a portion of a pin output capture cycle.

14. A method of testing an integrated circuit to determine whether boundary scan register (BSR) pin enable bit paths are not stuck in an "on" state, said method comprising:

loading desired circuit pin data and pin driver enable data into a BSR and updating said BSR;

loading opposite circuit pin data and opposite pin driver enable data into said BSR and suppressing updating of said register during a following update cycle of a test access port (TAP);

forcing output drivers into a high impedance state;

updating the data inputs to the output drivers to opposite logic values during one of a Run-test/idle or a Select-DR state of said TAP;

de-asserting a signal that tristates said drivers and then capturing pin logic values; and

unloading and comparing captured logic values with expected logic values to determine whether any pin enable bit path is stuck in an "on" state.

15. A method as defined in claim **14**, further including, prior to said loading opposite pin data, configuring the circuit in a test mode in which a pin tristating signal is de-asserted during a portion of a pin output capture cycle and BSR update is suppressed during a boundary scan update cycle and performed during a Run-test/idle or a Select-DR state of a circuit test access port.

16. A method of testing integrated circuits having a boundary scan register (BSR) to detect defects that might result in the flow of excess current, at least one integrated circuit having a tristate control circuit as defined in claim **1**, said method comprising:

tristating output pins of each said at least one integrated circuit having said tristate control circuit;

loading the BSR of all integrated circuits with values to force output drivers into desired output states;

capturing pin outputs into said BSR of all integrated circuits while de-asserting tristating only during a capture cycle of each said at least one integrated circuit; and

unloading captured data from said BSR of all integrated circuits and comparing captured data against expected values.

17. A method as defined in claim **16**, said steps of tristating, loading, capturing and unloading being performed using the IEEE1149.1 standard.